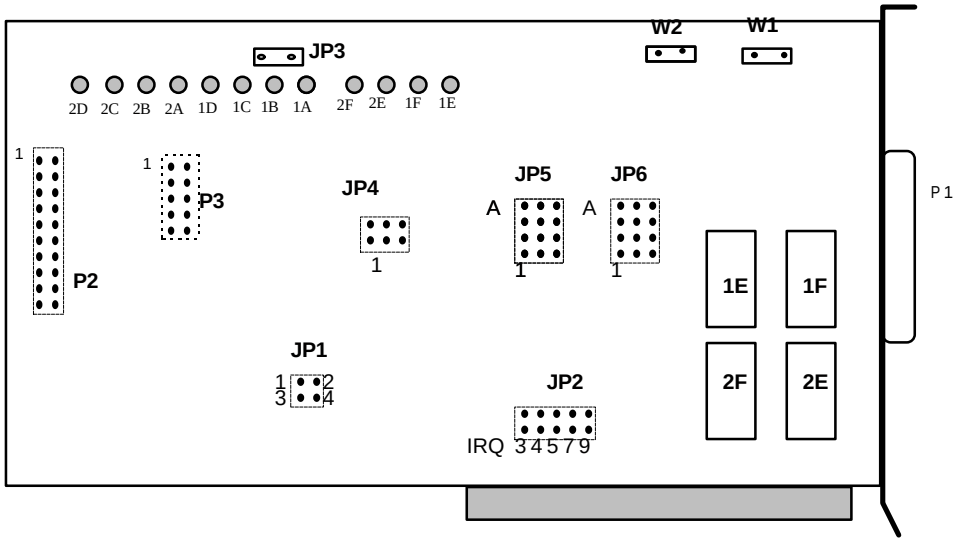
PIO-001
AC/DC Input/Output Interface Card

Rev. 1C (05-20-1997)

Specification and Application Notes



1. Features:

a) ISA 8-bit card to interface with two AC voltage inputs.
b) Three registers to store the input and output signals.
c) Port address is Jumper (JP1) selectable.
d) Interrupt Jumper (JP2) selectable, int-3,4,5,7,9.
e) Two high voltage input lines with Opto-isolator & D-flip flop to detect the AC or DC (20 - 120V) high voltage signals (W1,W2).
f) Six Opti-Isolator input lines for 3 - 10 VDC signals.
g) Four Relay sockets for using different type of Reed Relay (12- or 14- pin dip).
h) Four Relays provide four contacts or four voltage output lines (+5V or +12VDC).
i) Eight LEDs to indicate the Input status.
j) Four LEDs to indicate the Output status (software control only).
k) A 1x2 Jumper (JP3) to turn off the indication LED for saving energy.
l) A 2x3 Jumper (JP4) to select the polarity of input signals.
m) A 3x4 Jumper (JP5) to turn on the relay for testing.
n) A 3x4 Jumper (JP6) to supply Voltage to output lines.
o) A 2X10 Header (P2) for connecting to **PIO**002 Relay Card (8 relays).
p) A 2X5 Header (P3) for connecting to drive logic (8 output TTL signals).

2. LED Indicators:

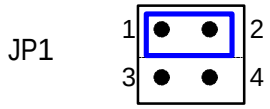
There are six LEDs for each lane, they are:

ID	LANE-1	LANE-2	I/O	Functional Example
A	GREEN	RED	INPUT	Foul Light
B	GREEN	RED	INPUT	Ball Indicator
C	GREEN	RED	INPUT	Reserved
D	GREEN	RED	INPUT	Reserved
E	GREEN	RED	OUTPUT	Pinsetter- 2nd Ball
F	GREEN	RED	OUTPUT	Pinsetter- Reset

* The output LEDs are controlled by software only.

3. Jumper Settings

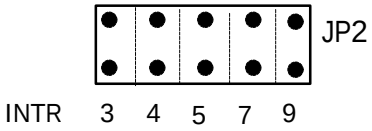
JP1: Port Address Selection



1-2	3-4	Base Port Address*
OFF	OFF	100h
OFF	ON	120h
ON	OFF	180h (default)
ON	ON	210h

* Base Addresses can be preprogrammed to any value between 100h to 3F0h. Please provide the information prior production.

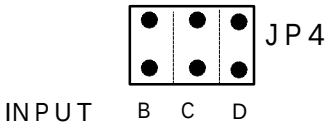
JP2: Interrupt Selection



3	4	5	7	9	Interrupt
OFF	OFF	OFF	OFF	OFF	None (default)
ON	OFF	OFF	OFF	OFF	3
OFF	ON	OFF	OFF	OFF	4
OFF	OFF	ON	OFF	OFF	5
OFF	OFF	OFF	ON	OFF	7
OFF	OFF	OFF	OFF	ON	9

* Only one shunt can be installed on JP2.

JP4: Input Source Polasrity 1B,1C,1D,2B,2C,2D lines.



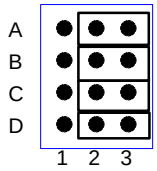
JP7	Active High	Active Low	Input Lines
1-2	OFF	ON	1B / 2B
3-4	OFF	ON	1C / 2C
5-6	OFF	ON	1D / 2D

W1: Input Source Jumper for Lane-1 Vac less than 40v.
W2: Input Source Jumper for Lane-2 Vac less than 40v.

W1, W2 setting:

Stay	Vac less than 40 volts
Remove (Default)	Vac greater than 40 volts

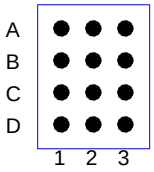
JP5: Relay Control Source Selection



A: Output-E for Lane-1;
B: Output-F for Lane-1;
C: Output-E for Lane-2;
D: Output-F for Lane-2.

1-2	2-3	Relay Control Source
OFF	OFF	Always OFF
ON	OFF	Always ON
OFF	ON	Software Latched Data (default)

JP6: Output Level Selection



A: Output-E for Lane-1;
B: Output-F for Lane-1;
C: Output-E for Lane-2;
D: Output-F for Lane-2.

1-2	2-3	Output Level
OFF	OFF	Contact Only (default)
ON	OFF	+12V
OFF	ON	+5V

Note: 1E,1F,2E,2F are independent to each other, their settings can be mixed.

WARNING: When using internal voltage to drive external device, the maximum current is 200 mA each, and must connect to OUT1Ey, OUT1Fy, OUT2Ey, or OUT2Fy pins. Do not connect any signal to OUT1Ex, OUT1Fx, OUT2Ex, or OUT2Fx pins.

---------- WARNING *** WARNING *** WARNING ----------

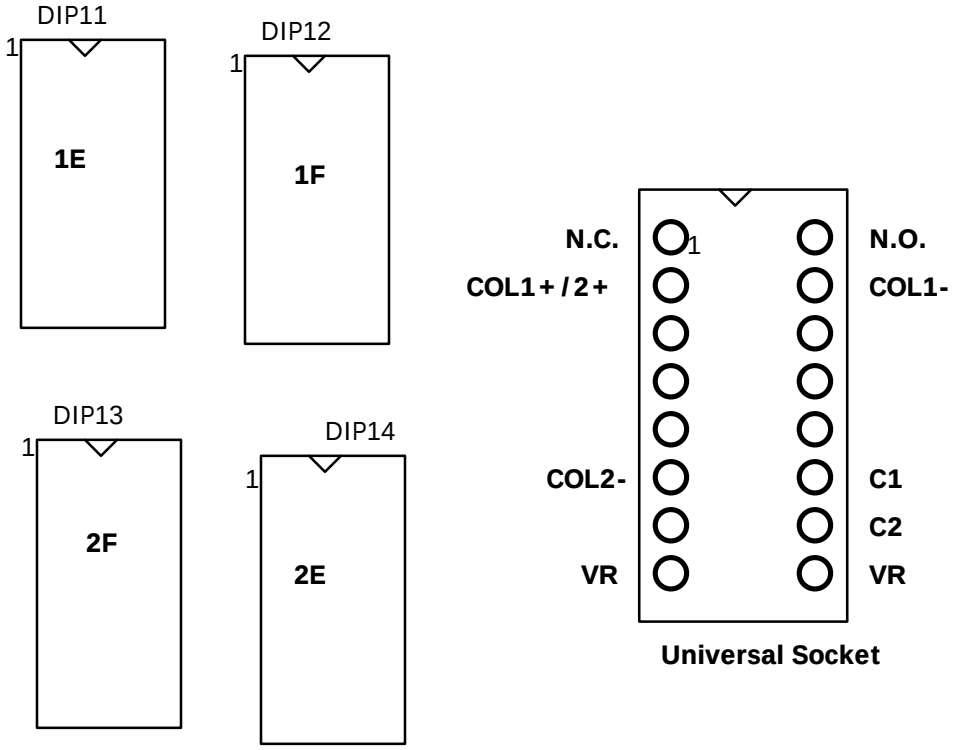
When apply High Voltage to PIO001 card:

a) To 1A or 2A directly, only while W1, W2 are removed.
b) To 1B,1C,1D,2B,2C,2D, only with a proper series resistor.
c) Only connect ?x pin (1Ex,1Fx,2Ex,2Fx) to external voltage source, while the related shunt on JP6 is removed.
d) Only connect ?y pin (1Ey,1Fy,2Ey,2Fy) to external device.

---------- WARNING *** WARNING *** WARNING ----------

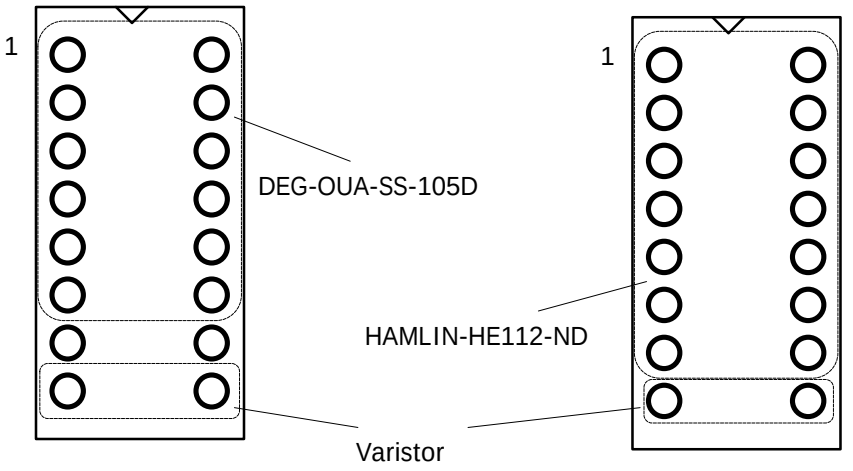
4. Relay Installation

Four sockets (DIP-16) are provided. Their locations and pin assignment are shown below.



Note: PCB Silkscreen 2E & 2F are swapped.

There are different type of Relay can be used. Two examples are shown below.



5. Software Commands

a) Read Input Status: Base Address + 0 ; DD = INP (&hxx0)

D7	D6	D5	D4	D3	D2	D1	D0
IN-D-2	IN-C-2	IN-B-2	IN-A-2	IN-D-1	IN-C-1	IN-B-1	IN-A-1

b) Write Output Latches-1: Base Address + 0 ; OUT &hxx0, DD

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	OUT-2F	OUT-2E	OUT-1F	OUT-1E

c) Write Output Latches-2: Base Address + 2 ; OUT &hxx2, DD

D7	D6	D5	D4	D3	D2	D1	D0
OUT-2K	OUT-2J	OUT-2H	OUT-2G	OUT-1K	OUT-1J	OUT-1H	OUT-1G

d) Clear Input Buffers: Base Address + 1 ; DD = INP(&hxx1)

e) Clear Output Latch-1: Base Address + 0 ; OUT &hxx0, 00
f) Clear Output Latch-2: Base Address + 2 ; OUT &hxx2, 00

g) For interrupt service, a Clear Input Buffers command is required to clear the Interrupt Request signal from latch. Otherwise, no more Interrupt Request can be issued.

6. DC Input Signal Polarity:

a) There are three TTL (0 to +5VDC) input lines for each lane, they are 1B, 1C, 1D, for lane-1 and 2B, 2C, 2D for lane-2.

b) The signal polarities of those TTL input lines are defined by JP4. When a jumper shunt is installed, the input signal must be Active Low, i.e., normally stays at high level.

*** Note: Pin-7 of P1 (DB25) supplies +5V.**

c) **WARNING:** Do not excess +10 v on those inputs. If a signal higher than 10 v. is needed, connect a series Resistor R_S, its resistance is determined as follows.

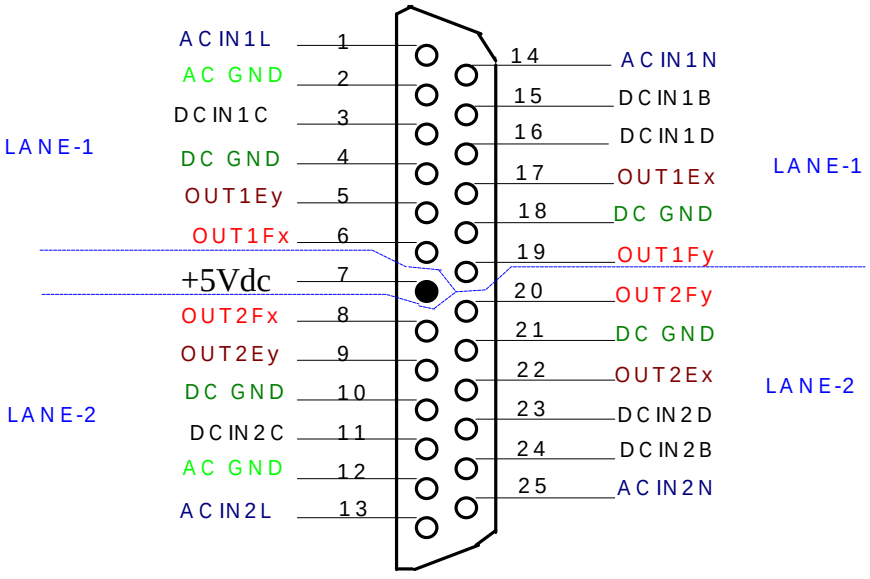
$$R_S = (V_{in} - 10) / 20 \quad \text{(in K-ohms)}$$

Where V_{in} is in unit of volts. For example, a 30VDC line needs Rs = 1K ohms.

6. I/O Connector (DB-25 Female) Pin Assignment:

Lane Number	Signals Name	DB-25 Pin Number	I/O	Function
1	ACIN1L	1	I	Foul Light (AC-Line or DC+)
1	ACIN1N	14	I	Foul Light (AC-Nu or DC-)
1	DCIN1B	15	I	Ball Indicator (max. +5VDC)
1	DCIN1C	3	I	Reserved (max. +5VDC)
1	DCIN1D	16	I	Reserved (max. +5VDC)
1	OUT1Ex	17	O	Pinsetter- 2nd Ball (Voltage Source or N/C)
1	OUT1Ey	5	O	Pinsetter- 2nd Ball (Solenoid)
1	OUT1Fx	6	O	Pinsetter- Reset (Voltage Source or N/C)
1	OUT1Fy	19	O	Pinsetter- Reset (Solenoid)
1	AC-GND	2	G	AC Ground
1	DC-GND	4,18	G	DC Ground
2	ACIN2L	13	I	Foul Light (AC-Line or DC+)
2	ACIN2N	25	I	Foul Light (AC-Nu or DC-)
2	DCIN2B	24	I	Ball Indicator (max. +5VDC)
2	DCIN2C	11	I	Reserved (max. +5VDC)
2	DCIN2D	23	I	Reserved (max. +5VDC)
2	OUT2Ex	22	O	Pinsetter- 2nd Ball (Voltage Source or N/C)
2	OUT2Ey	9	O	Pinsetter- 2nd Ball (Solenoid)
2	OUT2Fx	8	O	Pinsetter- Reset (Voltage Source or N/C)
2	OUT2Fy	20	O	Pinsetter- Reset (Solenoid)
2	AC-GND	12	G	AC Ground
2	DC-GND	10,21	G	DC Ground
1/2	Key	7	K	Protect Key

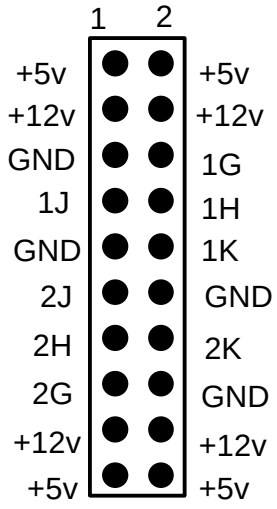
Note: Please check the settings of JP5 and JP6.



DB-25 Female

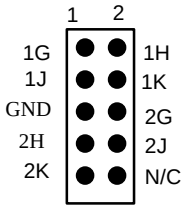
7. P2: PIO002 Interface Connector (2x10 Header) Pin Assignment:

To control the Relays 1G, 1H, 1J, 1K and 2G, 2H, 2J, 2K.



8. P3: TTL Output Connector (2x5 Header) Pin Assignment:

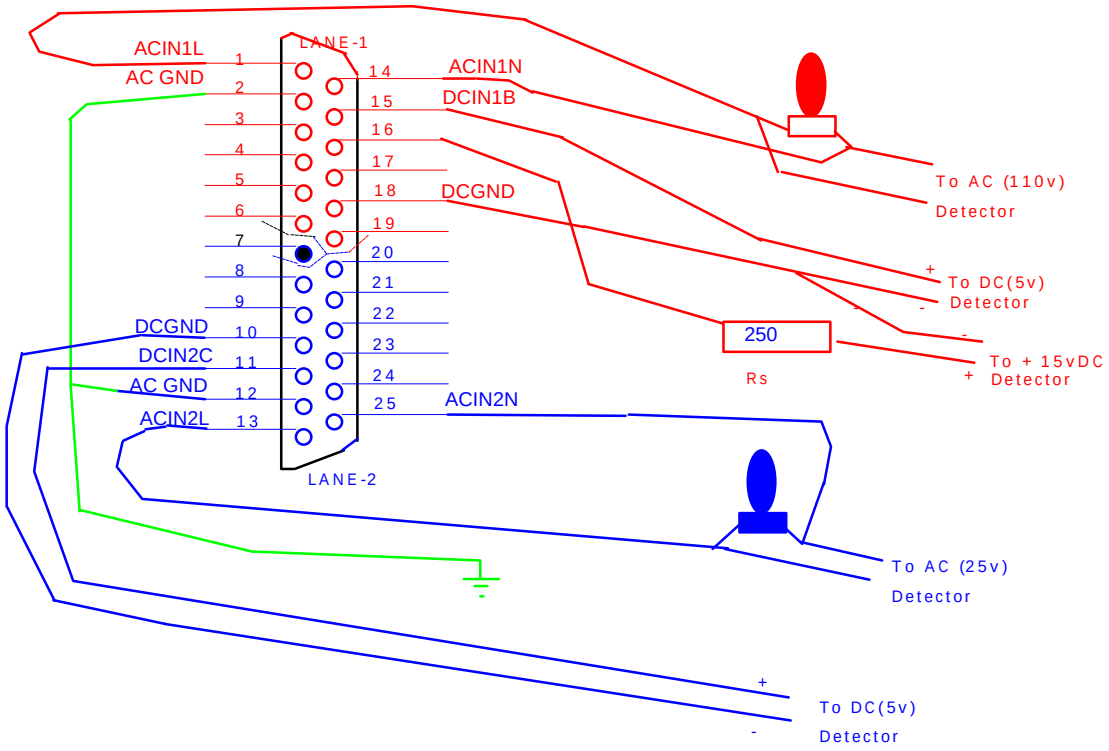
To control the Drive Logics for 1G, 1H, 1J, 1K and 2G, 2H, 2J, 2K. They are the reversed states of D0 ... D7.

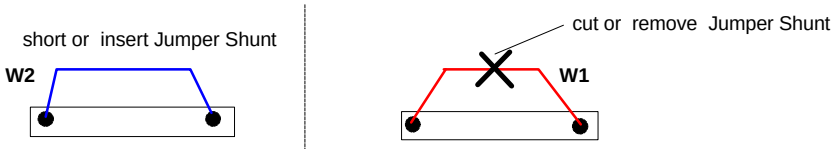


Note: P2, P3 are optional, U3 and U4 must be installed with 74LS175 to latch the data.

9. APPLICATION WIRING EXAMPLES:

a) Input Lines:





b) Output Lines: